

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION:      Frampton E. ELLIS, III      Conf. No.      7351  
SERIAL NUMBER:      09/085,755      Group:      2153  
FILED:      May 27, 1998      Examiner:      Sean REILLY  
FOR:      INTERNAL FIREWALLS FOR COMPUTERS AND  
MICROCHIPS (AS AMENDED)

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

Assistant Commissioner for Patents  
PO BOX 1450  
ALEXANDRIA, VA 22313-1450

April 2, 2007

Sir:

Applicant(s) wish(es) to disclose the following information.

REFERENCES

- ☒ Applicant(s) wish(es) to make of record the documents listed on the attached Form PTO-1449. Copies of the listed documents are attached, where required, as are either statements of relevancy or any readily available full or partial English translations of any non-English-language documents.

EXPLANATION OF RELEVANCE

RELATED CASES

- ☐ Attached is a list of Applicant's(s') pending applications and issued patents which may be related to the present application. Copies of the documents, where required, are attached along with Form PTO-1449.

CERTIFICATION

The undersigned certifies that

- ☐ each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign or international patent office in a counterpart foreign or international application for the first time (to the knowledge of the undersigned, having made reasonable inquiry) not more than three months prior to the filing of this statement (See 37 CFR 1.97(e)(1)).
- ☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign or international patent office in a counterpart foreign or international application, and, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement. (See 37 CFR 1.97(e)(2))

BASIS FOR CONSIDERATION

This Information Disclosure Statement is filed:

- ☐ without fee and within three months of the filing date of the application.
- ☐ without fee and within three months of the date of entry of the U.S. national stage.
- ☐ without fee and before the mailing date of a first Office Action on the merits (to the knowledge of the undersigned).
- ☐ without fee and with the appropriate certification above.
- ☐ without fee and with a new CPA application.
- ☒ without fee and with a Request for Continued Examination.
- ☐ with fee and before the mailing date of any Final Office Action, Notice of Allowance or an action that otherwise closes prosecution (to the knowledge of the undersigned).
- ☐ with fee, appropriate certification above, and before payment of the Issue Fee.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith, or credit any overpayment to Deposit Account No. 50-3266.

Respectfully submitted,

DLA PIPER US LLP



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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	09/085,755
				Filing Date	May 27, 1998
				First Named Inventor	Frampton E. ELLIS, III
				Art Unit	2153
				Examiner Name	Sean REILLY
Sheet	1	of	3	Attorney Docket Number	313449-P0005

## U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
		US -4,278,837	7/1/1981	Best	
		US -4,747,139	5/1/1988	Taaffe	
		US -5,862,357	1/19/1999	Hagersten et al.	
		US -6,167,428	12/26/00	Ellis	
		US -5,260,943	11/1993	Comroe et al.	
		US -5,615,127	3/1997	Beatty et al.	
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		US -5,600,597	2/1/1997	Kean et al.	
		US -5,809,190	9/1/1998	Chen	
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		US -6,732,141	5/1/2004	Ellis	
		US -6,287,949	9/1/2001	Mori et.al.	
		US -6,440,775	8/1/2002	Khoury	
		US -			
		US -			
		US -			
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## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
		EP 0 853 279	7/1998	Nagaratina et al.		
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Geppert, L. "Solid State [Trend/Development], IEEE Spectrum, v. 33, iss. 1, 1996, pp.51-55.	
		Li, Yao, "Free-space Optical Bus-based WDMA Interconnects for Parallel Computation", LEOS '92 Conference Proceedings, Lasers and Electron-Optics Society Annual Meeting, p. 588-589, Nov. 16-19, 1992.	
		Dickinson et al., "An Integrated Free Space Optical Bus", 1989 IEEE International Conference on Computer Design, VLSI In Computers and Processors, p. 62-65, October 2-4, 1989.	
		Natarajan et al., "Bi-Directional Optical Backplane Bus for General Purpose Multi-Processor", Journal of Lightwave Technology, Vol. 13, No. 6, p. 1031-1040, June 6, 1995.	
		Zhao et al., "General Purpose Bidirectional Optical Backplane: High Performance Bus for Multiprocessor Systems", Massively Parallel Processing Using Optical Interconnections, 2nd International Conference, p. 188-195, October 23-24, 1995.	
		Wu et al., "Microprocessor Control Signal Transmission Through Optical Fiber", Conference Record of 1992, IEEE Industry Applications Society Annual Meeting, p. 1747-1750, October 4-9, 1992.	
		Foster et al., "The Grid: Blueprint for a New Computing Infrastructure", Morgan Kaufman Publishers, Inc., 1998.	
		Hwang et al., "Scalable Parallel Computing", WCB McGraw-Hill, 1998.	
		Wilkinson, et al., "Parallel Programming", Prentice Hall, 1998.	
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		Patterson et al., "Computer Architecture: A Quantitative Approach" (2nd Edition), Morgan Kaufmann Publishers, Inc., 1996.	
		Culler et al., "Parallel Computer Architecture", Morgan Kaufmann Publishers, Inc., 1998.	
		Hennessy et al., "Computer Organization and Design", Morgan Kaufmann Publishers, Inc., 1998.	
		Slater, "The Microprocessor Today", IEEE Micro 1996, pp. 32-44.	
		Steinert-Threlkeld; "NEW BREED OF CHIP TI develops a super circuit"; The Sun Baltimore; May 4, 1992	
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		Mokhoff; "System-on-a-chip comes to wireless arena;" Electronic Engineering Times; Feb 12, 1996	
		Cindi; "System on a Chip' stars at ISSCC;" Electronic News; Feb 19, 1996	
		Ang; "System-on-a-chip to define next-generation set-top box"; Electronic Engineering Times; Dec 15, 1995	
		Marc; "New family of microprocessor cores from LSI Logic extends customers' system-on-a-chip design capability" Nov 7, 1994	
		Wall Street Journal; "Technology Brief - Advance Micro Devices Inc.: Company unveils Microchip for Hand-Held Computers"; Oct 18, 1993	
		Gelsinger, Patrick et al. "Microprocessors circa 2000," IEEE Spectrum, October 1989 pp. 43-47.	
		Yu, Albert. "The Future of Microprocessors," IEEE Micro, December 1996, pp. 46-53.	
		McWilliams. "Dell to Phase Out Computers Using Intel's Itanium," The Wall Street Journal, Online, September 15, 2005.	
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